

10

Fig. 1

FIG. 2 is a schematic diagram of a system 26, including a device 100, which is a memory device, and a controller 104, which is a microcontroller. The device 100 includes a memory array 106, which is a 4x4 array of memory cells. The controller 104 is connected to the memory array 106 via a bus 102. The system 26 is shown in a block diagram format, with the device 100 and controller 104 connected to a bus 102. The memory array 106 is shown as a 4x4 grid of memory cells, with each cell containing the hexadecimal value 'FF'.

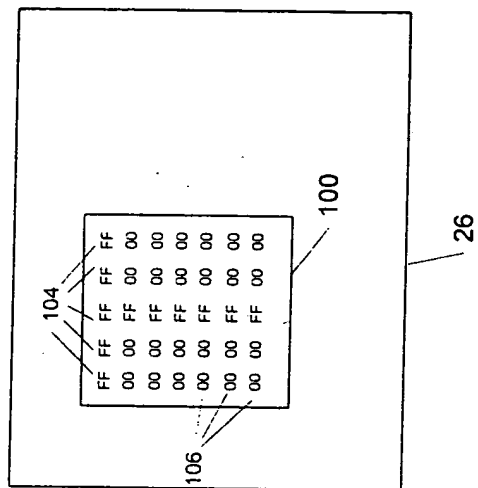


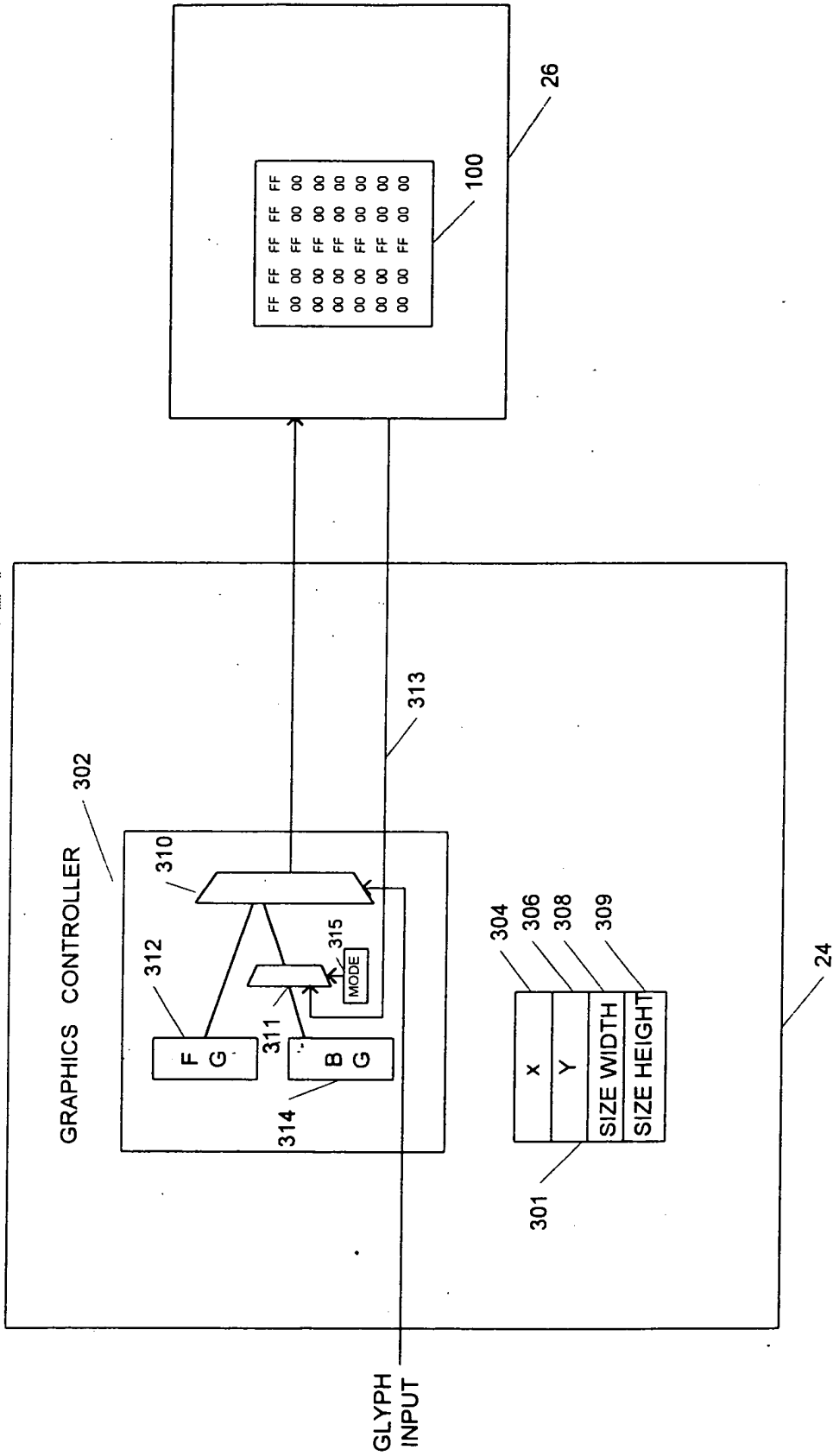
Fig. 2

1	1	1	1	1
0	0	1	0	0
0	0	1	0	0
0	0	1	0	0
0	0	1	0	0
0	0	1	0	0
0	0	1	0	0

300

Fig. 3

FIG. 4



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Fig. 4

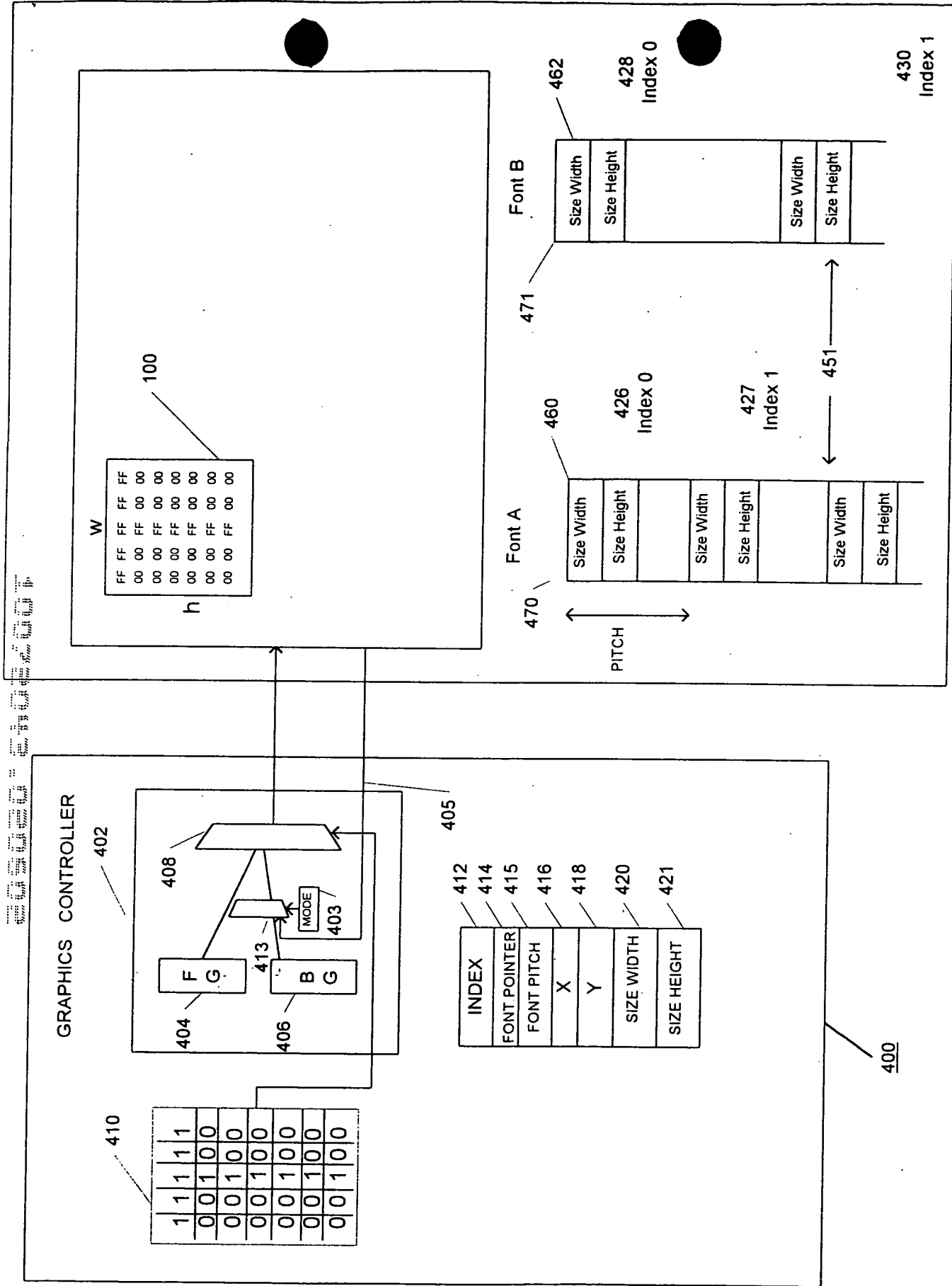


Fig. 5